AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-functional device comprising:

a bus;

a random access memory (RAM) coupled to said bus;

a central processing unit (CPU) coupled to said bus; and

a plurality of analog blocks coupled to said bus, wherein said bus, RAM, CPU and analog blocks reside on a single chip ~~in a single integrated circuit~~, said plurality of analog blocks comprising a first set of analog blocks that is ~~can be~~ selectively and electrically couplable ~~coupled~~ to and decouplable ~~decoupled~~ from another analog block in said plurality of analog blocks, wherein different analog functions are implemented by selectively and electrically coupling different combinations of said analog blocks; and

a plurality of configuration registers coupled to said plurality of analog blocks, wherein said analog blocks are selectively and electrically coupled according to information in said configuration registers.

2. (Original) The multi-functional device of Claim 1 wherein an analog block comprises a plurality of analog elements having changeable characteristics, wherein a characteristic of an analog element is specified according to said information in said configuration registers.

3. (Original) The multi-functional device of Claim 1 wherein said configuration registers are dynamically programmable.

4. (Original) The multi-functional device of Claim 1 wherein inputs and outputs of each analog block are specified according to said information in said configuration registers.

5. (Original) The multi-functional device of Claim 1 wherein said first set of analog blocks comprises switched capacitor blocks.

6. (Original) The multi-functional device of Claim 1 wherein said first set of analog blocks comprises a first type and a second type, wherein said first type is adapted to receive a first set of inputs and wherein said second type is adapted to receive a second set of inputs different from said first set of inputs.

7. (Original) The multi-functional device of Claim 1 wherein said plurality of analog blocks also comprises a second set of analog blocks, wherein said second set of analog blocks comprises continuous time blocks.

8. (Original) The multi-functional device of Claim 1 comprising:

a first register bank and a second register bank coupled to said plurality of configuration registers, said first register bank and said second register bank comprising addresses for said configuration registers.

9. (Original) The multi-functional device of Claim 8 wherein said first register bank is selected when a bit has a first value and said second register bank is selected when said bit has a second value.

10. (Currently Amended) An array of analog blocks comprising:

a first plurality of analog blocks comprising continuous time blocks;

a second plurality of analog blocks comprising switched capacitor blocks, said second plurality of analog blocks coupled to said first plurality of analog blocks, wherein a switched capacitor block is ~~can be~~ selectively and electrically coupled to and decoupled from another analog block to implement different analog functions and wherein said switched capacitor blocks comprise a first type and a second type, wherein said first type is adapted to receive a first set of inputs and wherein said second type is adapted to receive a second set of inputs different from said first set; and

a plurality of configuration registers coupled to said first plurality and said second plurality of analog blocks, wherein said first plurality and said second plurality of analog blocks are selectively and electrically coupled in different combinations according to information in said configuration registers.

11. (Original) The array of analog blocks of Claim 10 wherein an analog block comprises a plurality of analog elements having changeable characteristics, wherein a characteristic of an analog element is specified according to said information in said configuration registers.

12. (Original) The array of analog blocks of Claim 10 wherein said configuration registers are dynamically programmable.

13. (Original) The array of analog blocks of Claim 10 wherein inputs and outputs of each analog block are specified according to said information in said configuration registers.

14. (Canceled).

15. (Original) The array of analog blocks of Claim 10 wherein said configuration registers are coupled to a first register bank and a second register bank, said first register bank and said second register bank comprising addresses for said configuration registers.

16. (Original) The array of analog blocks of Claim 15 wherein said first register bank is selected when a bit has a first value and said second register bank is selected when said bit has a second value.

17. (Currently Amended) A multi-functional device comprising:

a plurality of analog blocks arranged in an array having multiple columns and rows, wherein an analog block comprises ~~comprising~~ a plurality of analog elements having changeable characteristics and wherein analog blocks in a column are each coupled to a digital bus; and

a configuration register coupled to said analog elements, wherein said configuration register comprises information for specifying characteristics of said analog elements and for selectively and electrically coupling said analog block to another analog block;

wherein different analog functions are implemented by changing said information in said configuration register.

18. (Original) The multi-functional device of Claim 17 wherein said configuration register is dynamically programmable.

19. (Original) The multi-functional device of Claim 17 wherein inputs and outputs of said analog block are specified according to information in said configuration register.

20. (Original) The multi-functional device of Claim 17 wherein said analog block is a switched capacitor block.

21. (Original) The multi-functional device of Claim 17 wherein said analog block is a continuous time block.

22. (Original) The multi-functional device of Claim 17 wherein said configuration register is coupled to a first register bank and a second register bank, said first register bank and said second register bank comprising an addresses for said configuration register.

23. (Original) The multi-functional device of Claim 22 wherein said first register bank is selected when a bit has a first value and said second register bank is selected when said bit has a second value.